

**Notice of References Cited**

Application/Control No.:

09/680,126

Applicant(s)/Patent Under  
Reexamination  
NEWLIN ET AL.

Examiner

Mary J. Steelman

Art Unit

2122

Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,450,586	09-1995	Kuzara et al.	717/124
	B	US-5,854,929	12-1998	Van Praet et al.	717/156
	C	US-5,870,588	02-1999	Rompaey et al.	703/13
	D	US-5,896,521	04-1999	Shackleford et al.	703/21
	E	US-6,142,683	11-2000	Madduri, Venkateswara Rao	717/128
	F	US-2001/0025363	09-2001	Ussery et al.	716/1
	G	US-2001/0032305	10-2001	Barry, Edwin F.	712/34
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Hogl, H., Kugel, A., Ludvig, J., Manner, R., Noffz, K.H., Zoz, R., "Enable ++: A Second Generation FPGA Processor", 1995 IEE p. 45-53, retrieved from IEEE database 05/01/2003.
	V	Kirovski, Darko, Lee, Chunho, Potkonjak, Miodrag, Mangione-Smith, William H., "Application-driven Synthesis of Memory-Intensive Systems-on-Chip", 1999 IEEE, p. 1316-1326, retrieved from IEEE database 05/01/2003.
	W	Winegarden, Steven, "A Bus Architecture Centric Configurable Processor System", 1999 IEEE, p. 627-630, retrieved from IEEE database 05/01/2003.
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.